	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 20040240588 A1	20041202	65	Compensation for non-linear distortion in a modem receiver	375/340	375/350	Miller, William J.
2	US 20030177409 A1	20030918	31	Self-timed pipeline for tunable delays	713/401		Greenstreet, Mark R.
3	US 20030133514 A1	20030717	50	Apparatus and method for decode arbitration in a multi-stream multimedia system	375/260		Lais, Eric et al.
4	US 20030081705 A1	20030501	39	Compensation for non-linear distortion in a modem receiver	375/346		Miller, William J.
5	US 20020130944 A1	20020919	49	Light-emission modulation having effective scheme of creating gray scale on image	347/132	347/248	Ema, Hidetoshi et al.
6	US 6754746 B1	20040622	42	Memory array with read/write methods	710/100	365/206; 365/230.01; 365/230.03; 365/233; 710/305; 710/307; 711/103; 711/151; 714/759	Leung; Wingyu et al.

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7	US 6735264 B2	20040511	38	Compensation for non-linear distortion in a modem receiver	375/340	329/319; 329/320; 375/349; 375/350; 455/303; 455/307; 455/43; 455/501	Miller; William J.
8	US 6731317 B2	20040504	48	Pulse modulation signal generation circuit, and semiconductor laser modulation device, optical scanning device and image formation device using the same	347/135	347/132	Ema; Hidetoshi et al.
9	US 6690309 B1	20040210	28	High speed transmission system with clock inclusive balanced coding	341/102	341/50	James; David Vernon et al.
10	US 6388587 B1	20020514	22	Partial response channel having combined MTR and parity constraints	341/59	714/802	Brickner; Barrett J. et al.

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11	US 6359525 B1	20020319	15	Modulation technique for transmitting multiple high data rate signals through a band limited channel	332/108	329/312; 329/313; 332/109; 332/112; 370/212; 370/213; 375/238; 375/239; 375/242; 375/340	Mohan; Chandra et al.
12	US 6356555 B1	20020312	110	Apparatus and method for digital data transmission using orthogonal codes	370/441	370/442; 370/478; 370/479; 370/480; 370/503	Rakib; Selim Shlomo et al.
13	US 6288668 B1	20010911	56	Analog to digital converter, encoder, and recorded data reproducing apparatus	341/172	341/159	Tsukamoto; Sanroku et al.
14	US 6281721 B1	20010828	12	Programmable frequency divider	327/115	327/117; 327/147	Kinget; Peter R. et al.

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15	US 6154456 A	20001128	43	Apparatus and method for digital data transmission using orthogonal codes	370/342	370/350; 370/479; 370/508; 370/528	Rakib; Selim Shlomo et al.
16	US 5991308 A	19991123	161	Lower overhead method for data transmission using ATM and SCDMA over hybrid fiber coax cable plant	370/395.53	370/342; 370/395.52; 370/395.65; 370/474	Fuhrmann; Amir Michael et al.
17	US 5966376 A	19991012	41	Apparatus and method for digital data transmission using orthogonal cyclic codes	370/342	370/441; 370/479; 375/261; 375/298; 375/358; 714/746; 714/795; 725/144	Rakib; Selim Shlomo et al.

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18	US 5805583 A	19980908	45	Process for communicating multiple channels of digital data in distributed systems using synchronous code division multiple access	370/342	370/335; 370/347; 370/441; 370/479; 375/261; 375/298; 375/358	Rakib; Selim Shlomo
19	US 5793759 A	19980811	65	Apparatus and method for digital data transmission over video cable using orthogonal cyclic codes	370/342	370/441; 725/111; 725/126	Rakib; Selim Shlomo et al.
20	US 5786732 A	19980728	26	Phase locked loop circuitry including a multiple frequency output voltage controlled oscillator circuit	331/1A	327/105; 327/116; 327/159; 331/177 R; 331/34; 331/57; 331/74	Nielson; Edward T.
21	US 5768269 A	19980616	43	Apparatus and method for establishing frame synchronization in distributed digital data communication systems	370/342	370/441; 370/508; 370/509	Rakib; Selim Shlomo et al.
22	US 5745837 A	19980428	76	Apparatus and method for digital data transmission over a CATV system using an ATM transport protocol and SCDMA	725/114	725/129; 725/131	Fuhrmann; Amir Michael

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23	US 5646557 A	19970708	7	Data processing system and method for improving performance of domino-type logic using multiphase clocks	326/97	326/96; 326/98	Runyon; Stephen Larry et al.
24	US 5321750 A	19940614	84	Restricted information distribution system apparatus and methods	380/230	348/476; 380/240; 725/109; 725/25; 725/37	Nadan; Joseph S.
25	US 4105995 A	19780808	186	Digitally controlled transmission impairment measuring apparatus	714/714	379/28	Bothof; Delwin L. et al.

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1	US 20050021925 A1	20050127	15	Accessing in parallel stored data for address translation	711/203	711/212	Clark, Lawrence T. et al.
2	US 20040237024 A1	20041125	70	Robust signal transmission in digital television broadcasting	714/784		Limberg, Allen LeRoy
3	US 20040196231 A1	20041007	74	Liquid crystal display device with influences of offset voltages reduced	345/87		Goto, Mitsuru et al.
4	US 20040022112 A1	20040205	31	HIGH VOLTAGE PULSE METHOD AND APPARATUS FOR DIGITAL MULTILEVEL NON-VOLATILE MEMORY INTEGRATED SYSTEM	365/226		Tran, Hieu Van et al.
5	US 20040003309 A1	20040101	13	Techniques for utilization of asymmetric secondary processing resources	713/320		Cai, Zhong-Ning et al.
6	US 20030201918 A1	20031030	41	Method and apparatus for adaptive bus coding for low power deep sub-micron designs	341/50		Henkel, Jorg et al.
7	US 20030152051 A1	20030814	21	High data rate CDMA wireless communication system	370/332		Odenwalder, Joseph P.
8	US 20030133423 A1	20030717	64	Octave pulse data method and apparatus	370/330		LaDue, Christoph
9	US 20030106011 A1	20030605	208	Decoding device	714/780		Miyauchi, Toshiyuki et al.
10	US 20030088821 A1	20030508	207	Interleaving apparatus	714/788	714/701	Yokokawa, Takashi et al.
11	US 20030061003 A1	20030327	205	Soft-output decoder	702/181		Miyauchi, Toshiyuki et al.
12	US 20030014700 A1	20030116	26	Method and apparatus for interleaving, deinterleaving and combined interleaving-deinterleaving	714/701		Giulietti, Alexandre et al.
13	US 20020186597 A1	20021212	40	Method and apparatus for adaptive address bus coding for low power deep sub-micron designs	365/200		Henkel, Jorg et al.

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14	US 20020114388 A1	20020822	43	Decoder and decoding method, recorded medium, and program	375/240.01		Ueda, Mamoru et al.
15	US 20020110154 A1	20020815	21	High data rate CDMA wireless communication system	370/503	370/329	Odenwalder, Joseph P.
16	US 20020036942 A1	20020328	93	Semiconductor integrated circuit device having a hierarchical power source configuration	365/226		Ooishi, Tsukasa
17	US 20020009096 A1	20020124	20	HIGH DATA RATE CDMA WIRELESS COMMUNICATION SYSTEM	370/441	370/342	ODENWALDER, JOSEPH P.
18	US 20010040834 A1	20011115	93	Semiconductor integrated circuit device having a hierarchical power source configuration	365/226		Ooishi, Tsukasa
19	US 6788608 B2	20040907	30	High voltage pulse method and apparatus for digital multilevel non-volatile memory integrated system	365/226	365/189.09; 365/227	Tran; Hieu Van et al.
20	US 6741190 B2	20040525	39	Method and apparatus for adaptive bus coding for low power deep sub-micron designs	341/50	341/51	Henkel; Jorg et al.
21	US 6678843 B2	20040113	28	Method and apparatus for interleaving, deinterleaving and combined interleaving-deinterleaving	714/701	714/786	Giulietti; Alexandre et al.
22	US 6622307 B1	20030916	25	Multiple-room signal distribution system	725/120	725/121; 725/149; 725/71; 725/78; 725/80; 725/82	Ho; Kesse
23	US 6583735 B2	20030624	39	Method and apparatus for adaptive bus coding for low power deep sub-micron designs	341/51	712/300	Henkel; Jorg et al.

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24	US 6574161 B2	20030603	82	Semiconductor integrated circuit device having a hierarchical power source configuration	365/226	365/189.07; 365/189.09; 365/210; 365/227	Ooishi; Tsukasa
25	US 6560744 B1	20030506	23	Method and device for detecting rate	714/774		Burshtein; David
26	US 6549525 B2	20030415	23	High data rate CDMA wireless communication system	370/332	370/335; 370/342	Odenwalder; Joseph P.
27	US 6408421 B1	20020618	50	High-speed asynchronous decoder circuit for variable-length coded data	714/795	714/791	Benes ; Martin et al.
28	US 6396804 B2	20020528	23	High data rate CDMA wireless communication system	370/209	370/342	Odenwalder; Joseph P.
29	US 6351406 B1	20020226	42	Vertically stacked field programmable nonvolatile memory and method of fabrication	365/103	365/164	Johnson; Mark G. et al.
30	US 6327213 B1	20011204	82	Semiconductor integrated circuit device having a hierarchical power source configuration	365/226	365/189.07; 365/189.09; 365/210; 365/227	Ooishi; Tsukasa
31	US 6288668 B1	20010911	56	Analog to digital converter, encoder, and recorded data reproducing apparatus	341/172	341/159	Tsukamoto; Sanroku et al.
32	US 6188806 B1	20010213	23	Apparatus for reading optical data from a motion picture film and a light source therefor	382/312	352/27; 369/125	Inatome; Kiyoshi et al.
33	US 6112325 A	20000829	32	Method and device for detecting rate	714/774	714/780; 714/795	Burshtein; David
34	US 6028972 A	20000222	23	Apparatus for reading optical data from a motion picture film and a light source therefor	382/312	352/27; 369/125	Inatome; Kiyoshi et al.

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35	US 5898677 A	19990427	11	Integrated circuit device having a switched routing network	370/276	257/210; 257/499; 326/17; 340/2.1; 370/537	Deeley; Richard et al.
36	US 5761349 A	19980602	22	Apparatus for reading optical data from a motion picture film and a light source therefor	382/312	352/27; 369/125	Inatome; Kiyoshi et al.
37	US 5719819 A	19980217	89	Semiconductor storage circuit device operating in a plurality of operation modes and corresponding device for designing a semiconductor storage circuit device	365/230.06	365/230.05	Maeno; Hideshi
38	US 5675365 A	19971007	18	Ejector activation scheduling system for an ink-jet printhead	347/9	347/14	Becerra; Juan J. et al.
39	US 5615126 A	19970325	12	High-speed internal interconnection technique for integrated circuits that reduces the number of signal lines through multiplexing	716/1		Deeley; Richard et al.
40	US 5467315 A	19951114	81	Semiconductor memory device facilitated with plural self-refresh modes	365/222	365/233; 365/236	Kajimoto; Takeshi et al.
41	US 5311476 A	19940510	82	Semiconductor memory, components and layout arrangements thereof, and method of testing the memory	365/222	331/186; 331/57	Kajimoto; Takeshi et al.
42	US 5161120 A	19921103	82	Data output buffer for a semiconductor memory	365/189.05	365/203	Kajimoto; Takeshi et al.
43	US 4463339 A	19840731	12	State/interval redundant controller system for traffic signals	340/906	340/642; 340/916; 340/931; 701/117	Frick; Ralph E. et al.

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44	US 4385398 A	19830524	50	Selective call communication receiver	340/7.49	340/7.33; 340/825.73; 455/227; 455/343.2; 455/702	Wycoff; Keith H. et al.
45	US 4322842 A	19820330	24	Broadcast system for distribution automation and remote metering	370/204	340/825.72; 370/206; 370/210; 370/312; 455/353	Martinez; Louis
46	US 4128894 A	19781205	8	Bubble domain circuit organization	365/4	365/12; 365/14	Chen; Thomas T.
47	US 4051998 A	19771004	25	Digital electronic data system for a fluid dispenser	705/413	222/23; 377/21; 377/47	Zabel; William P.
48	US 4051388 A	19770927	7	Flip-flop accompanied by two current switches, one having a smaller current sink capability than the other	327/213	326/106; 365/154; 365/203; 365/205	Inukai; Hidemori
49	US 4007451 A	19770208	13	Method and circuit arrangement for operating a highly integrated monolithic information store	365/154	365/190; 365/205; 365/227	Heuber; Klaus et al.
50	US 3962686 A	19760608	16	Memory circuit	365/233	326/106; 326/97; 365/182	Matsue; Shigeki et al.

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51	US 3941924 A	19760302	16	Simplified multi-channel data sensor system	375/240.01	341/143; 370/532; 375/247	Leiboff; Teague N.
52	US 3788058 A	19740129	10	ELECTRONIC DIGITAL CLOCK APPARATUS	368/87	968/904; 968/955; 968/DIG .1	Idei; Gijun et al.
53	US 3784976 A	19740108	11	MONOLITHIC ARRAY ERROR DETECTION SYSTEM	714/802	148/DIG .37; 148/DIG .85; 257/563; 326/42; 714/804	Ho; Irving T.

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1	US 20040042566 A1	20040304	16	Symbol reliability determination and symbol pre-selection based on reliability criteria	375/341		Eidson, Donald Brian et al.
2	US 20030128777 A1	20030710	25	Decision directed phase locked loops (DD-PLL) with multiple initial phase and/or frequency estimates in digital communication systems	375/327	375/376	Linsky, Stuart T. et al.
3	US 20030123595 A1	20030703	16	Multi-pass phase tracking loop with rewind of future waveform in digital communication systems	375/376	375/341	Linsky, Stuart T. et al.
4	US 20030112914 A1	20030619	16	Multi-pass phase tracking loop with rewind of current waveform in digital communication systems	375/376		Linsky, Stuart T. et al.
5	US 20030112899 A1	20030619	26	Decision directed phase locked loops (DD-PLL) with excess processing power in digital communication systems	375/327	327/156; 329/307; 375/376	Linsky, Stuart T. et al.
6	US 20030103582 A1	20030605	24	Selective reed-solomon error correction decoders in digital communication systems	375/327		Linsky, Stuart T. et al.
7	US 20030054755 A1	20030320	20	Wireless receiver with anti-jamming	455/1	455/403	Zehavi, Ephraim et al.
8	US 20030043925 A1	20030306	25	Method and system for detecting, timing, and correcting impulse noise	375/254		Stopler, Danny et al.
9	US 6781447 B2	20040824	15	Multi-pass phase tracking loop with rewind of current waveform in digital communication systems	329/304	329/307; 375/324; 375/326; 375/329; 375/376	Linsky; Stuart T. et al.

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10	US 6690739 B1	20040210	53	Method for intersymbol interference compensation	375/265	375/285; 375/348; 714/792	Mui; Shou Yee
11	US 6625233 B1	20030923	11	Method and apparatus in a wireless receiver for demodulating a continuous-phase frequency-shift-keyed signal	375/334	375/232	Carsello; Stephen Rocco
12	US 6470047 B1	20021022	28	Apparatus for and method of reducing interference in a communications receiver	375/232	375/350	Kleinerman; Alexander et al.
13	US 5968198 A	19991019	13	Decoder utilizing soft information output to minimize error rates	714/752	714/751; 714/755; 714/780	Hassan; Amer A. et al.
14	US 5966401 A	19991012	26	RF simplex spread spectrum receiver and method with symbol deinterleaving prior to bit estimating	375/150	370/209	Kumar; Derek D.
15	US 5862186 A	19990119	21	RF simplex spread spectrum receiver and method	375/324	375/142; 375/340	Kumar; Derek D.
16	US 5717723 A	19980210	10	Apparatus for use in equipment providing a digital radio link between a fixed radio unit and a mobile radio unit	375/340	714/807	Hulbert; Anthony Peter